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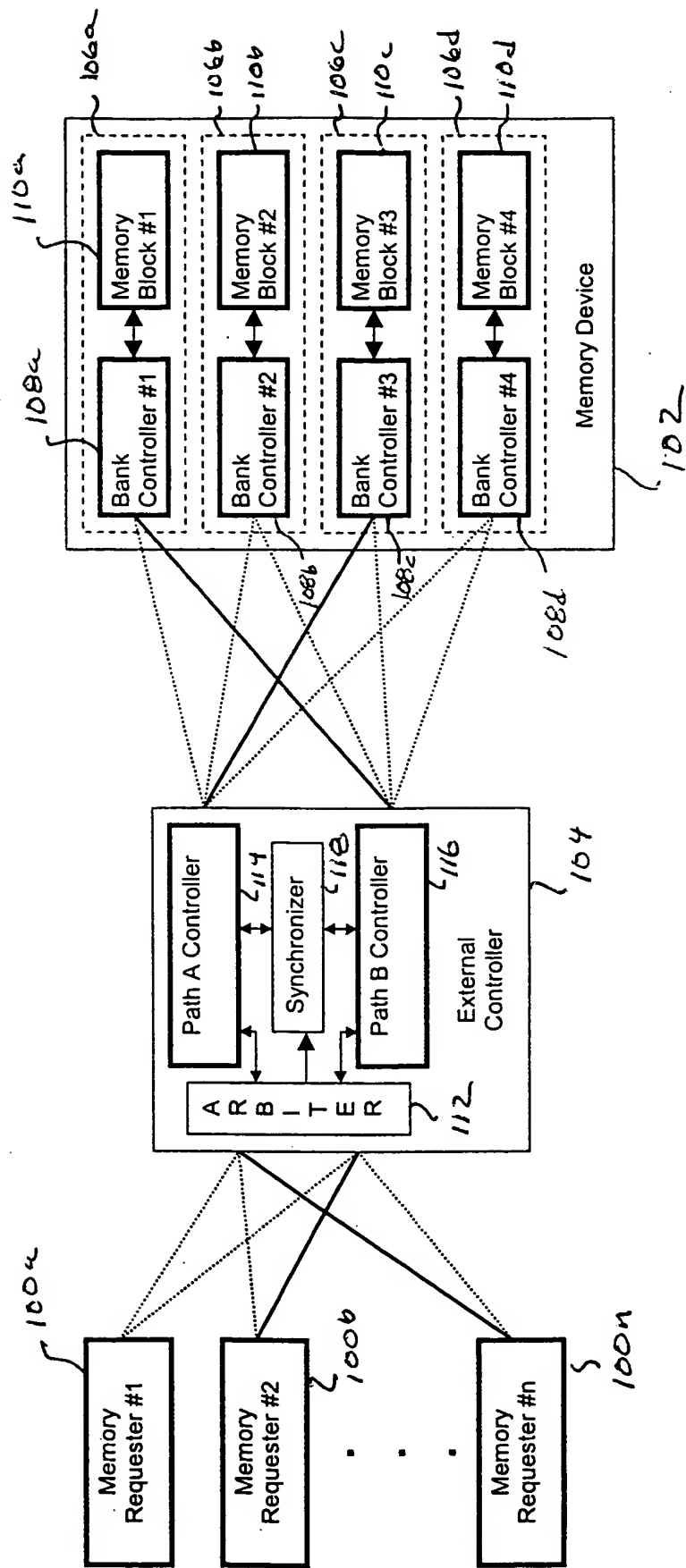


FIG. 1

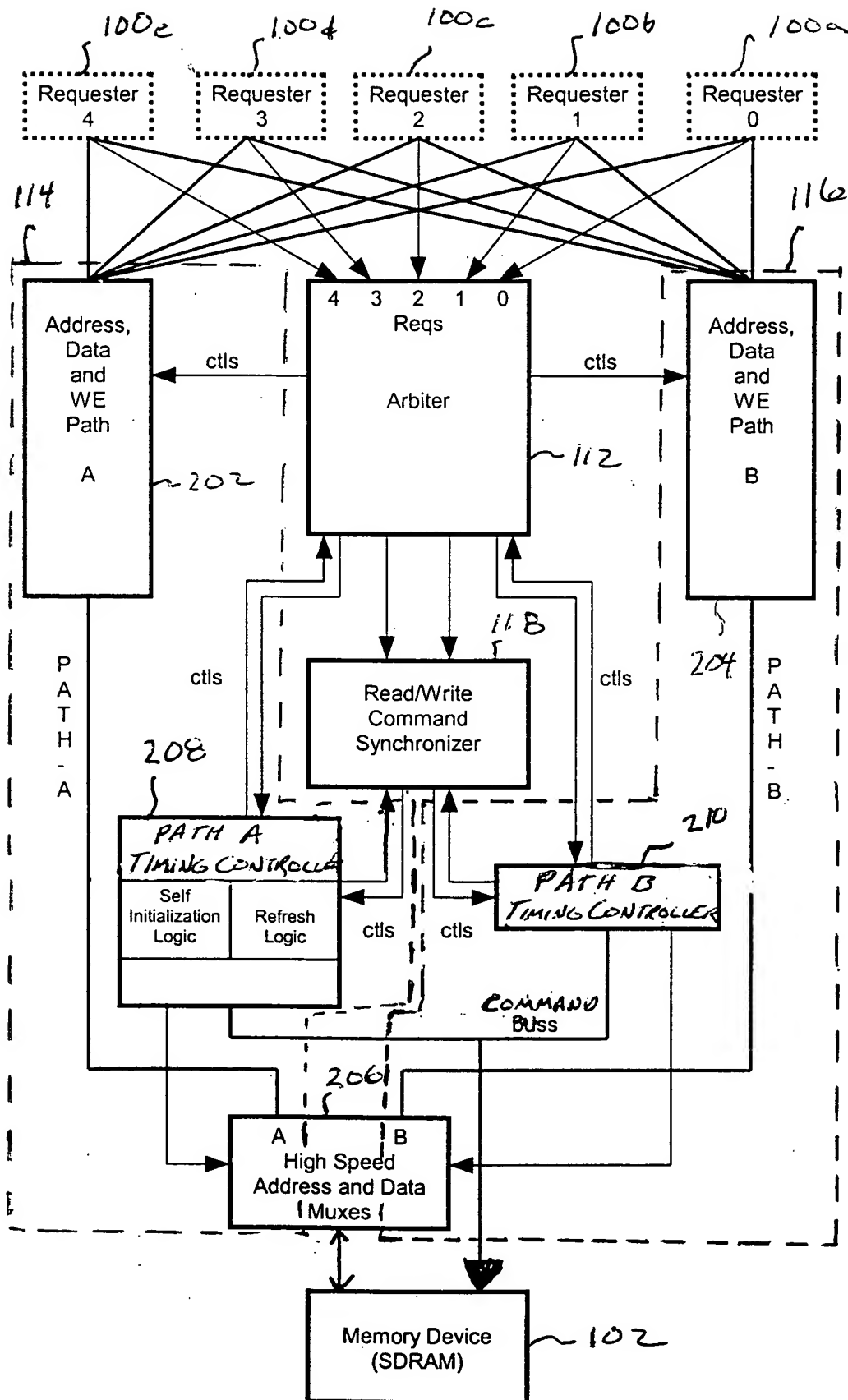
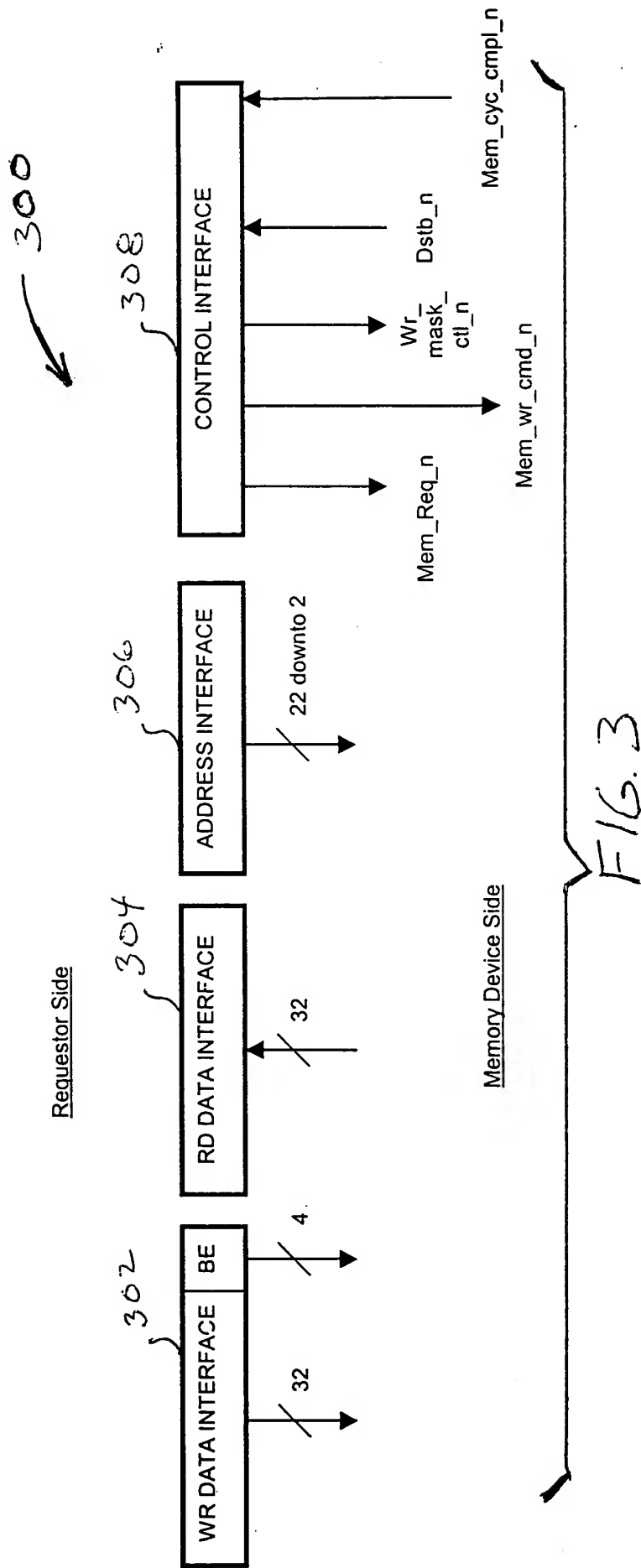


FIG. 2



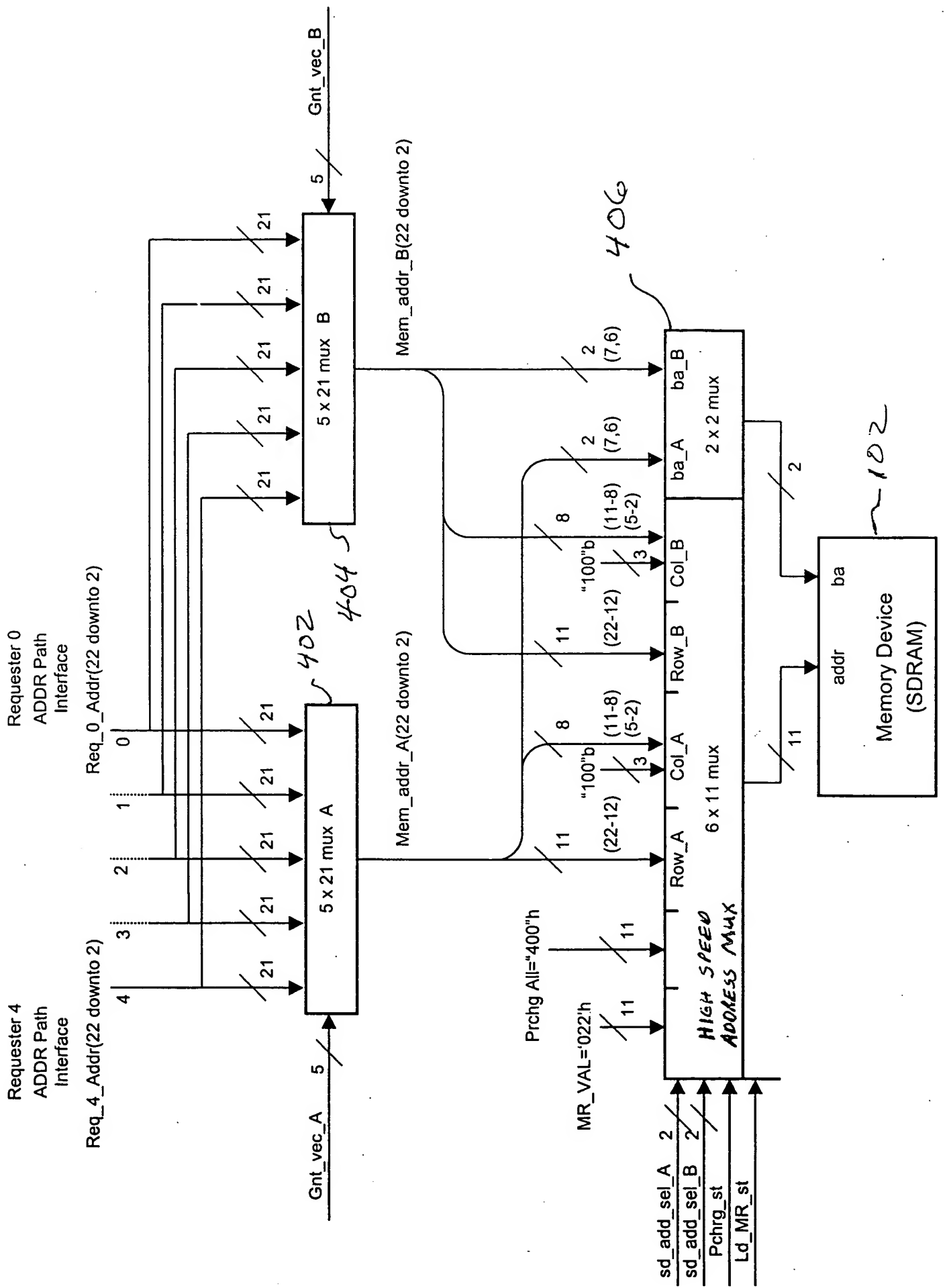


FIG. 4

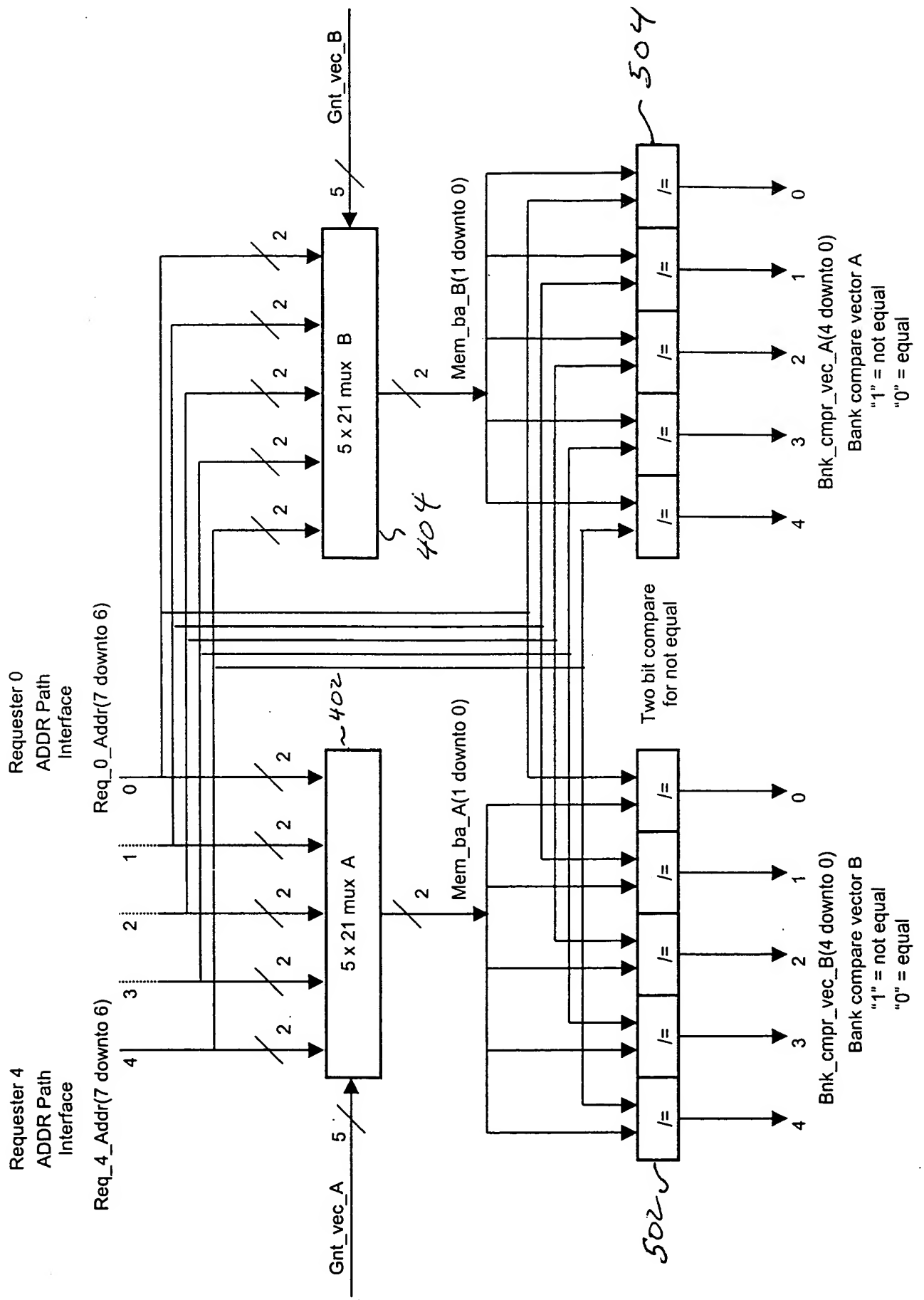


FIG. 5

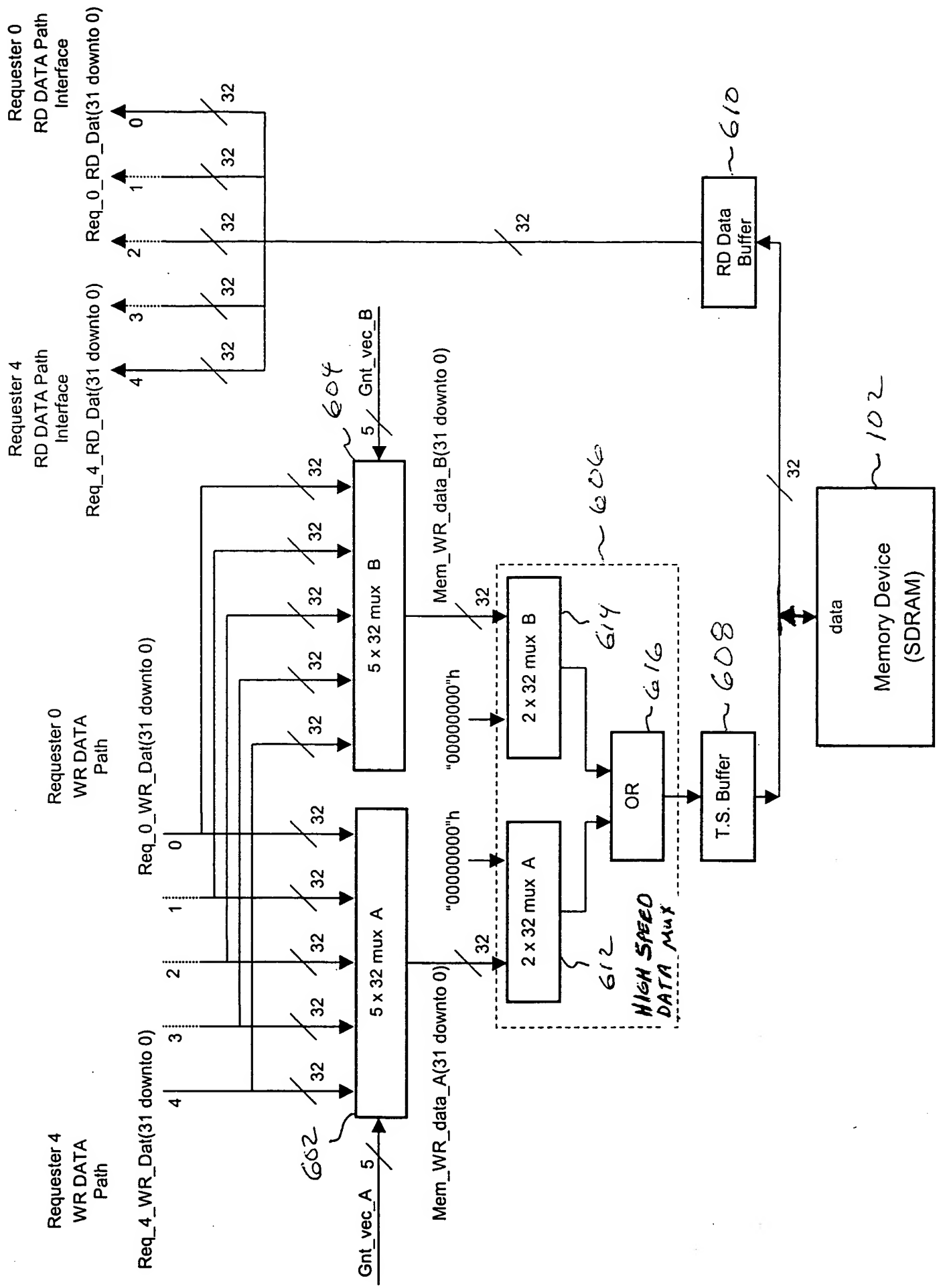


FIG. 6

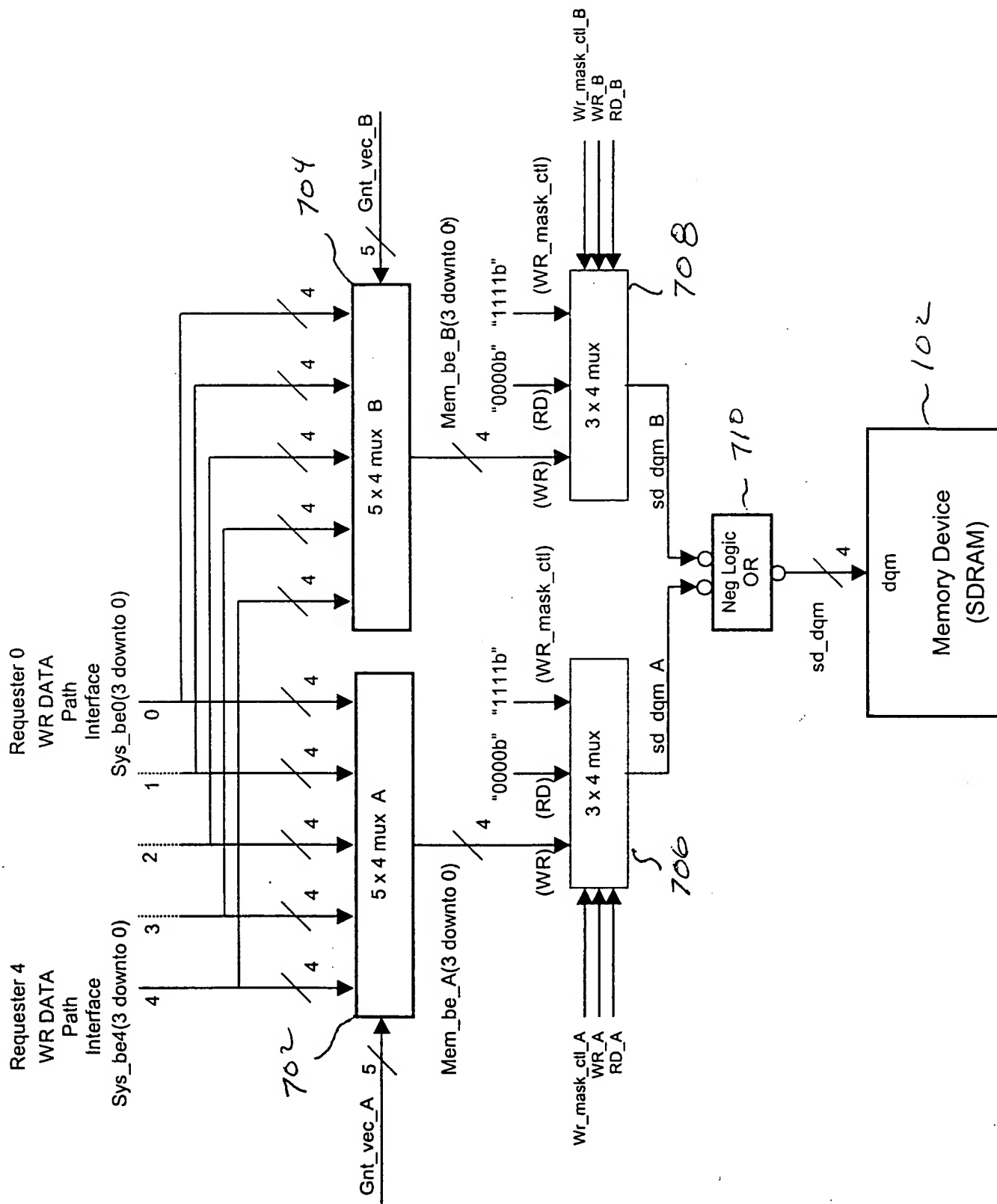


FIG. 7

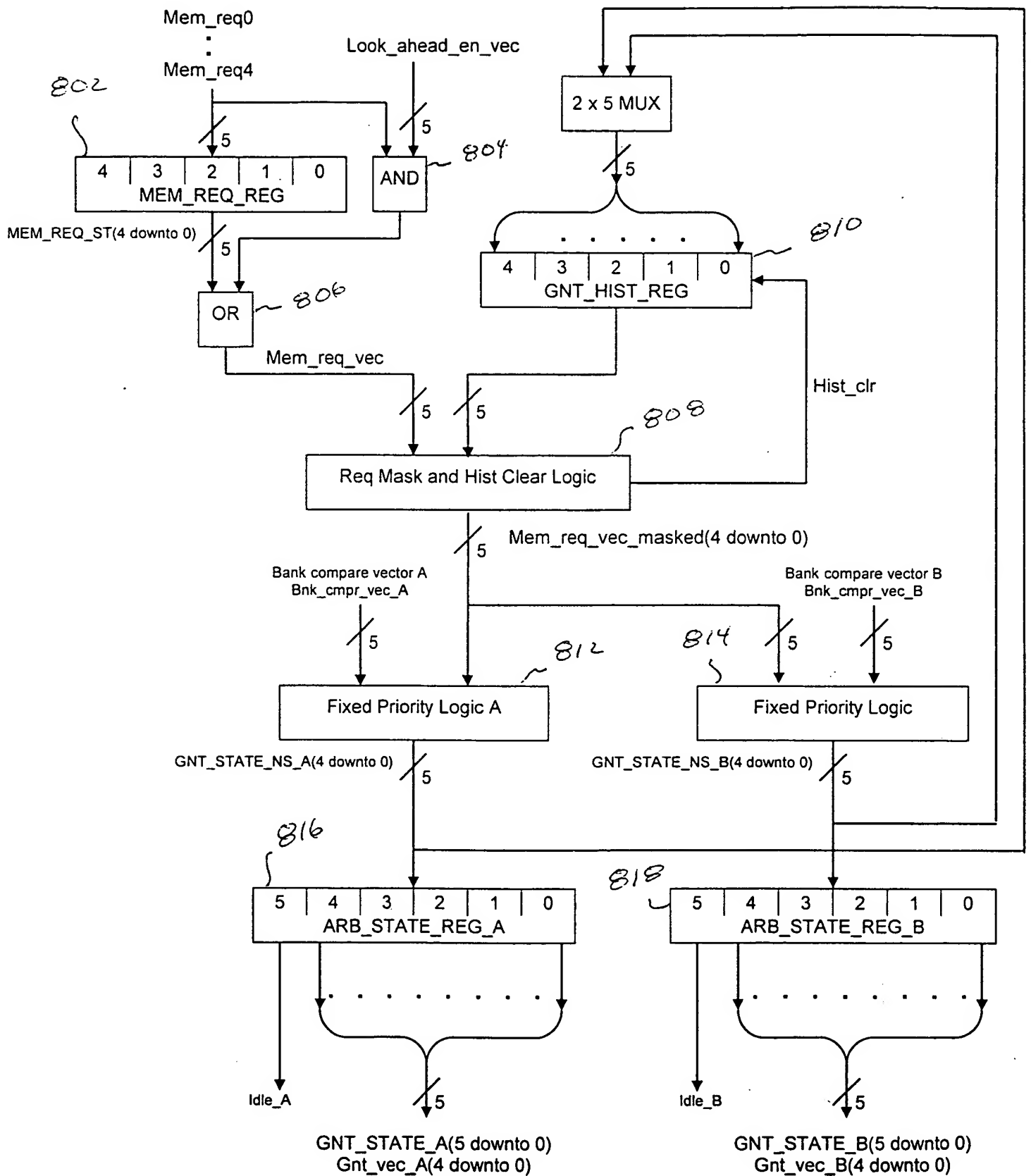


FIG 8

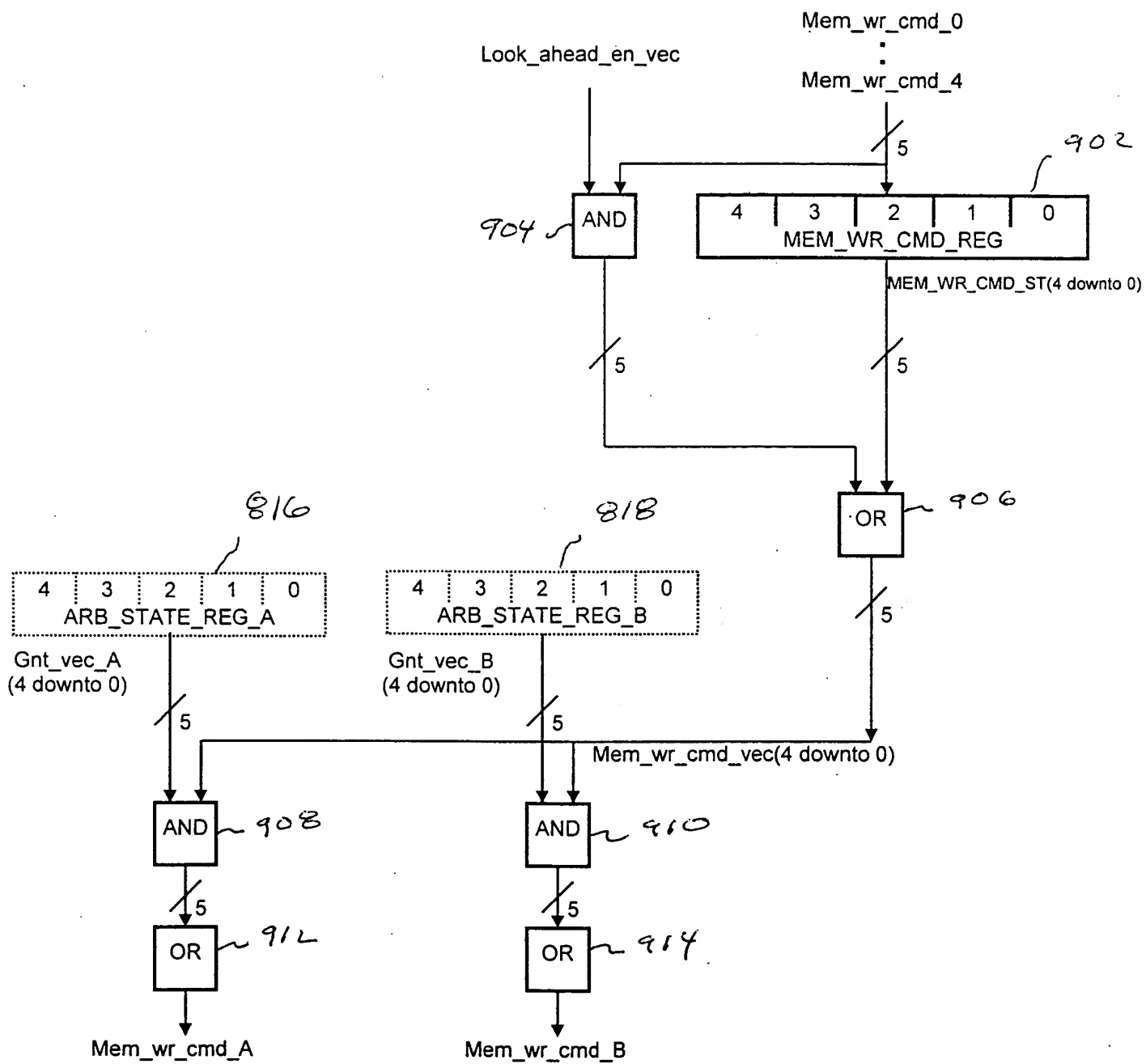


FIG 9

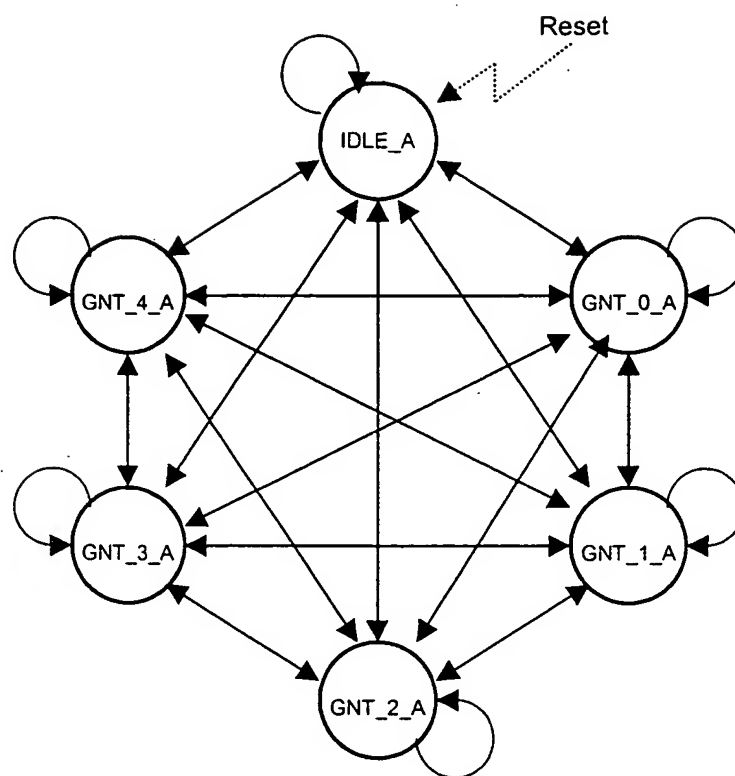


FIG. 10A

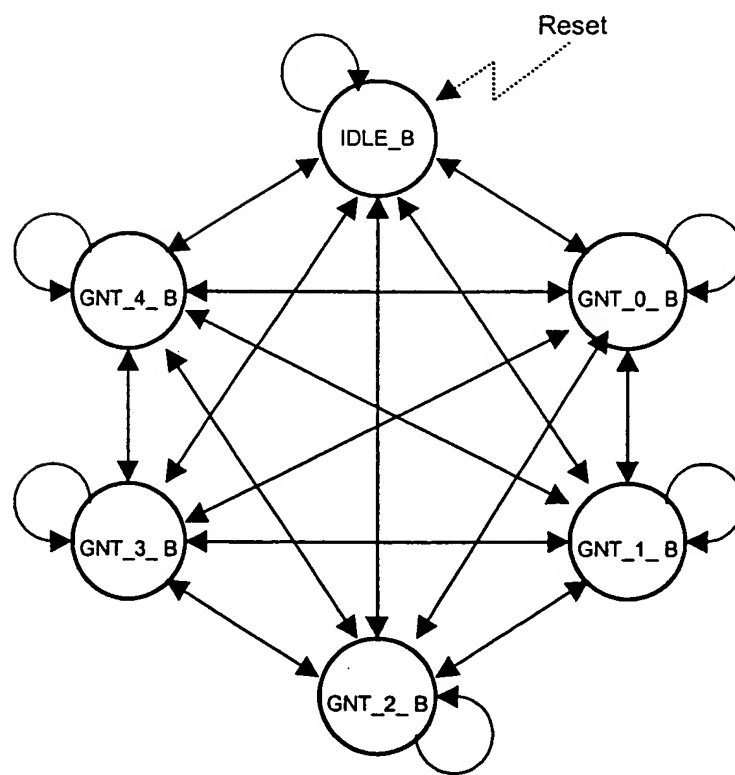


FIG. 10B

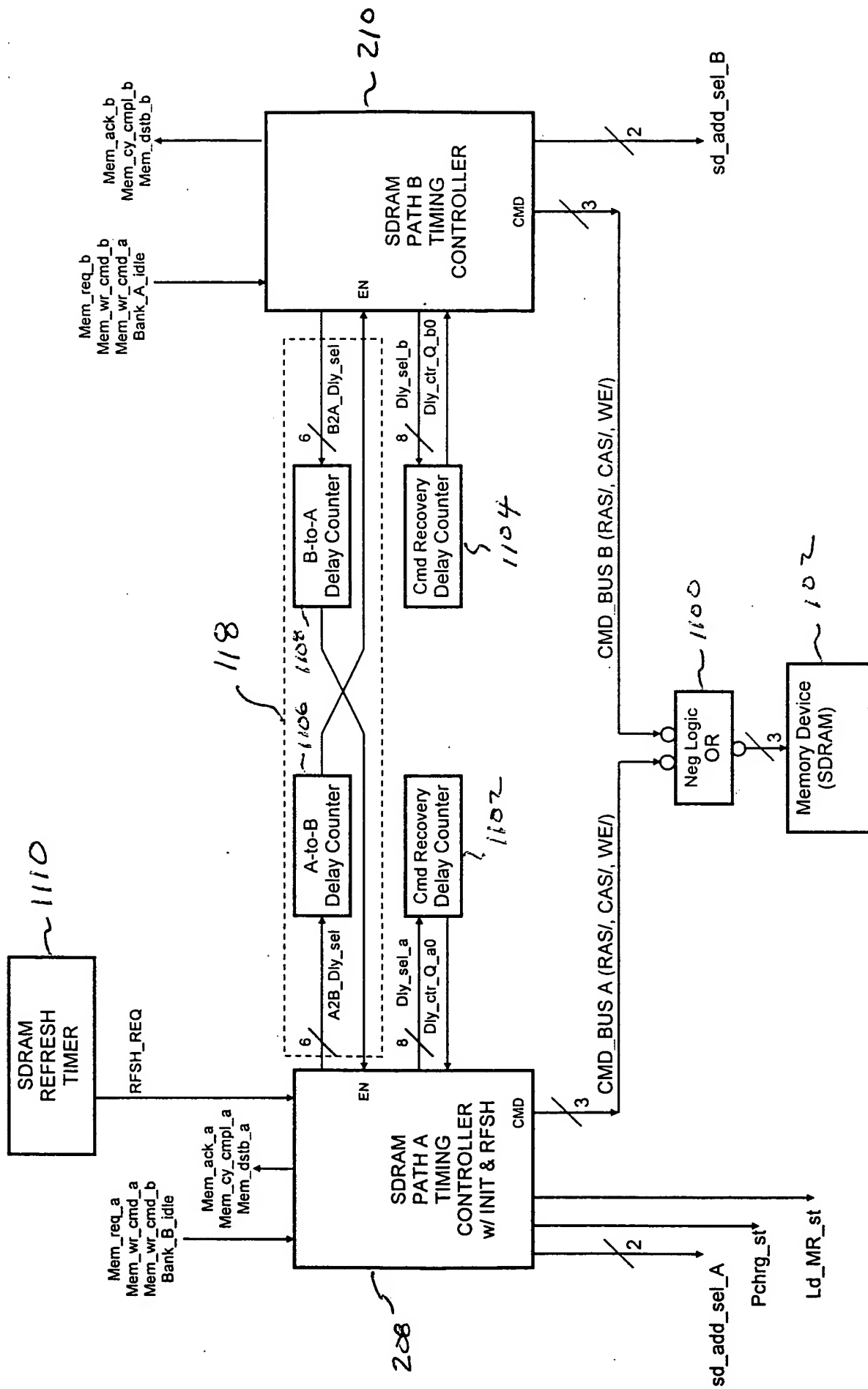


FIG. 11

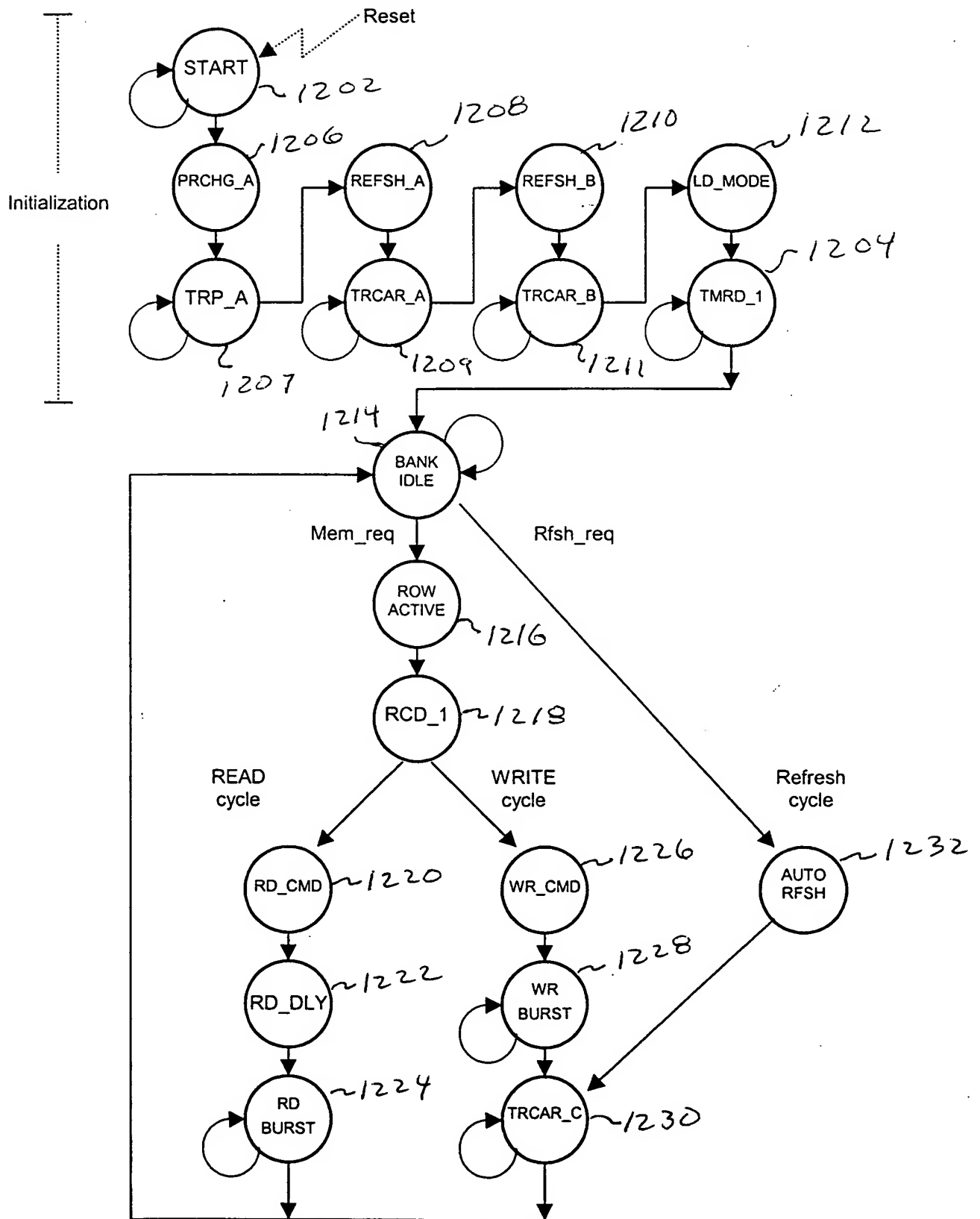


FIG. 12

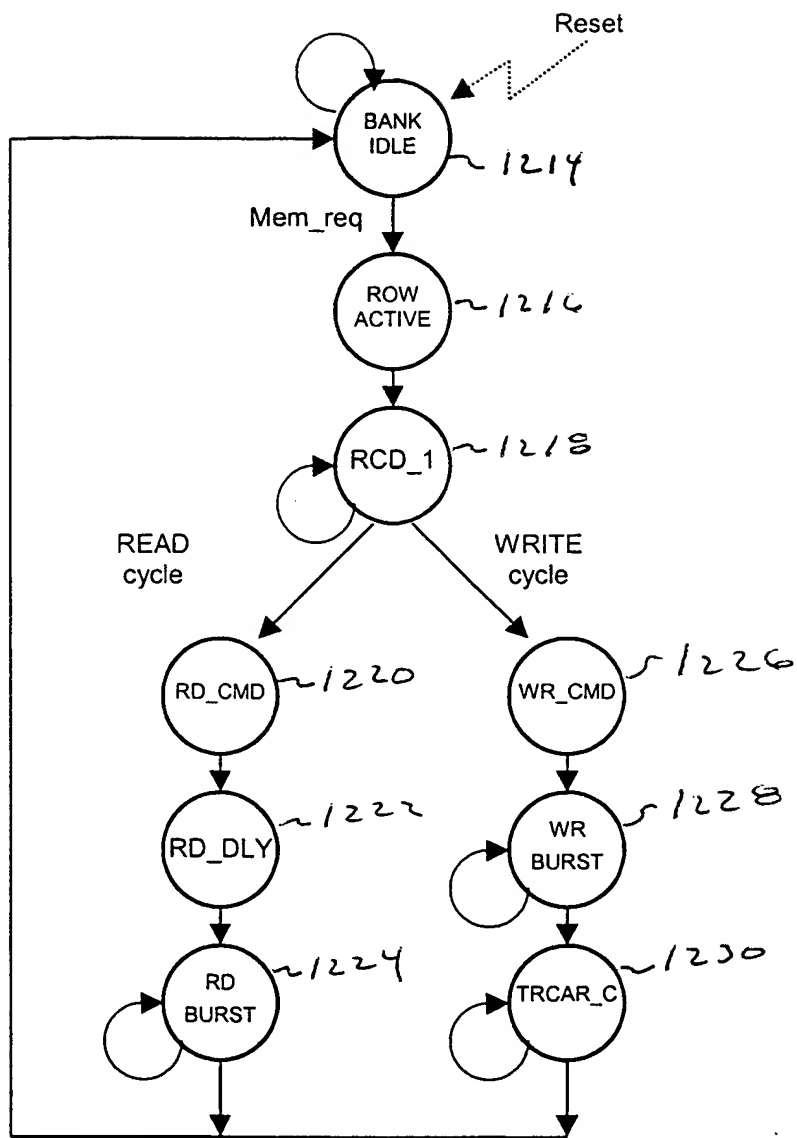


FIG. 13

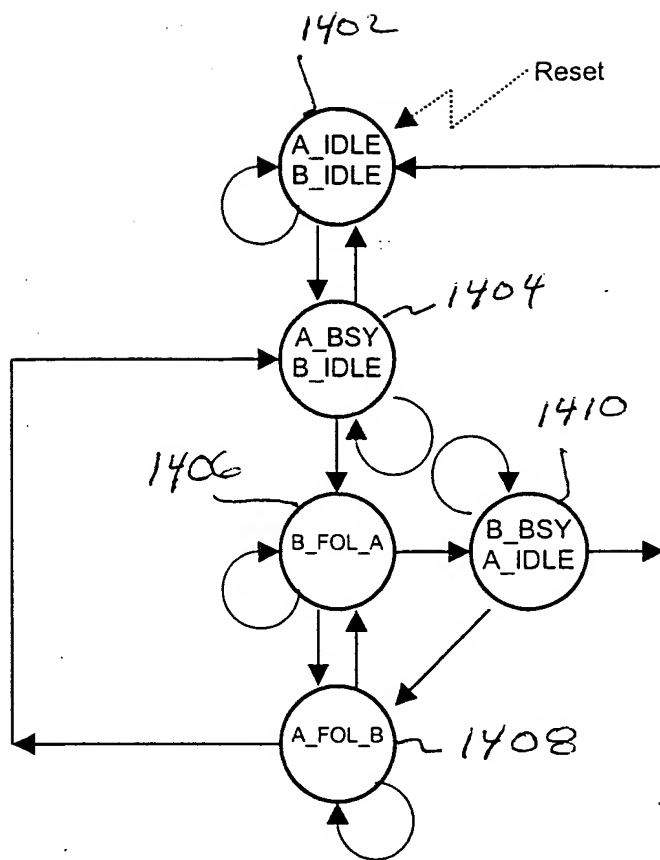


FIG. 14

SINGLE BANK SDRAM TIMINGS

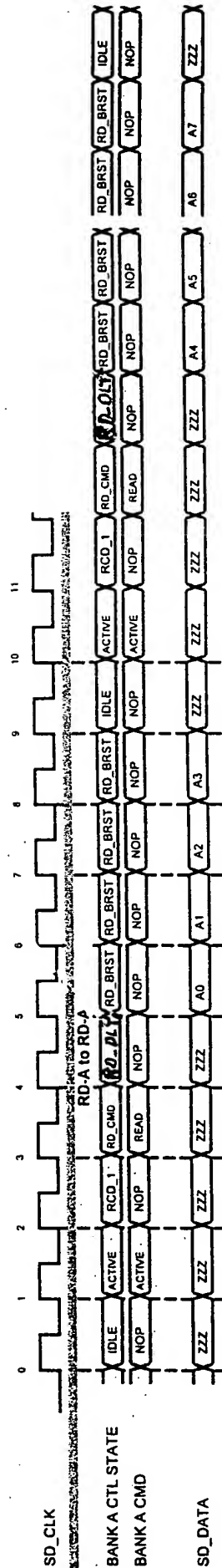


FIG. 15A

SINGLE BANK SDRAM TIMINGS

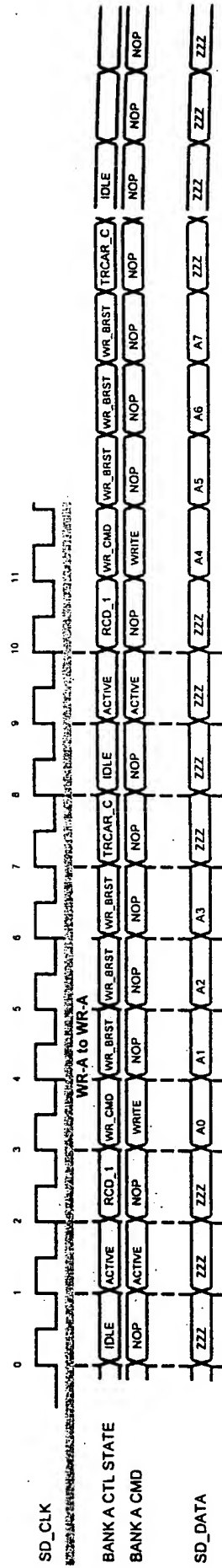
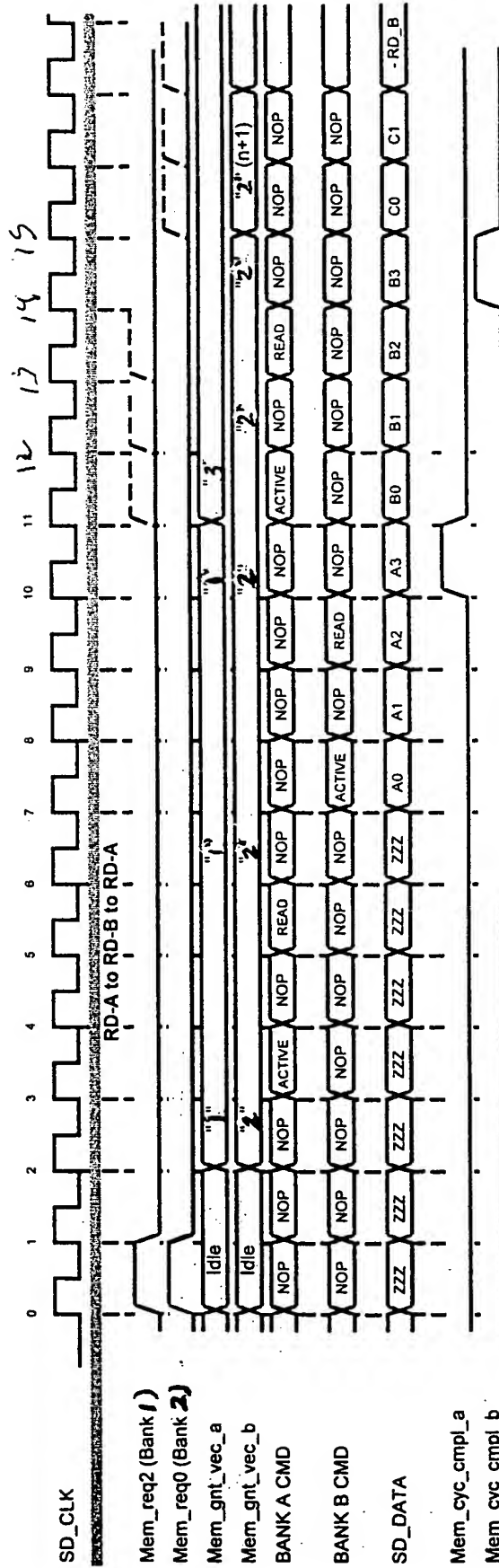


FIG. 15D

TWO BANK SDRAM TIMINGS



F16. Kakt

TWO BANK SDRAM TIMINGS

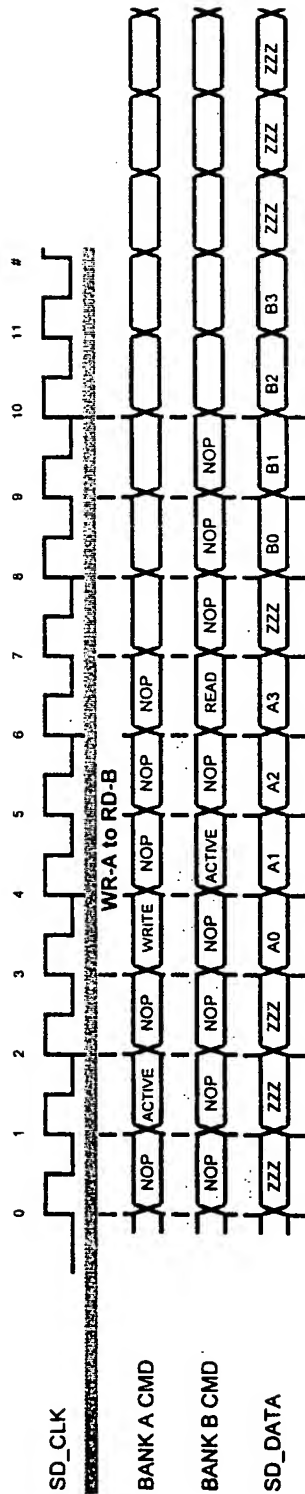


FIG. 160

TWO BANK SDRAM TIMINGS

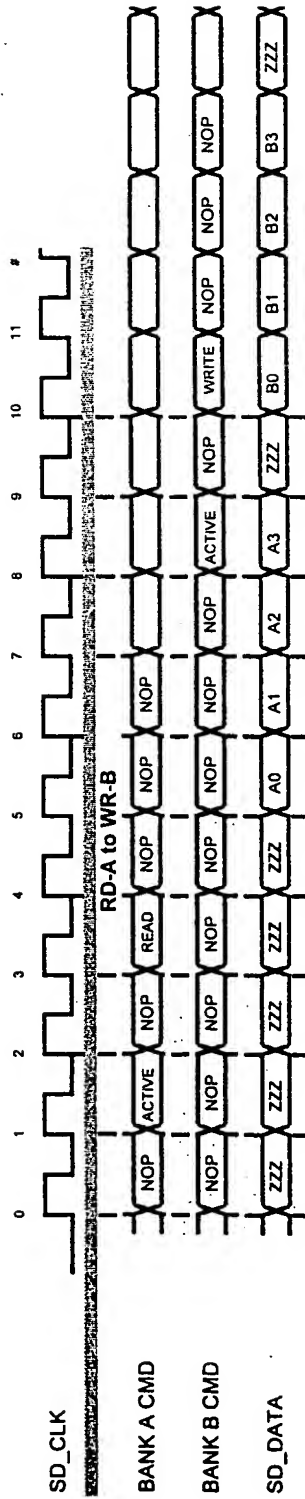


FIG. 16C

TWO BANK SDRAM TIMINGS

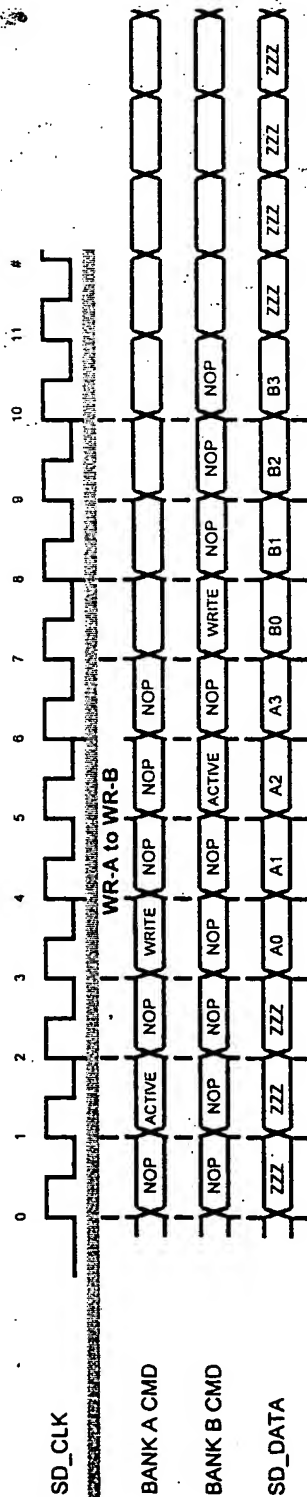


FIG. 16D